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Institute of Computing Technology,Chinese Academy of Sciences

A Virtual Channel Mechanism For Memory Controller Design in Multicore Era

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Abstract

We propose virtual channel mechanism, a novel memory controller optimization technique, to provide dedicated channels between memory controller and processes that run on multicore processors simultaneously.

Reverse-TLB (RTLB) is added into memory controller to reverse physical address to process id (pid) and virtual address. The virtual channel mechanism exposes memory controller to operating system.

Initial experimental results show that, with virtual channel mechanism, memory controller can explore up to 33% more spatial regularity than traditional memory controller.

1 Insights

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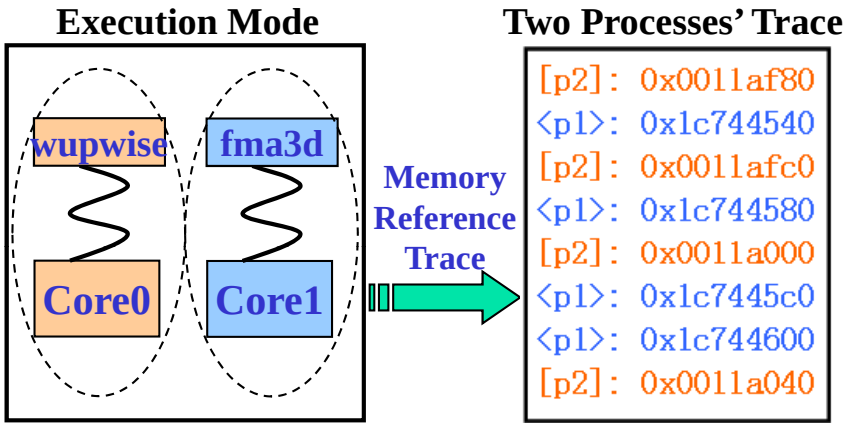
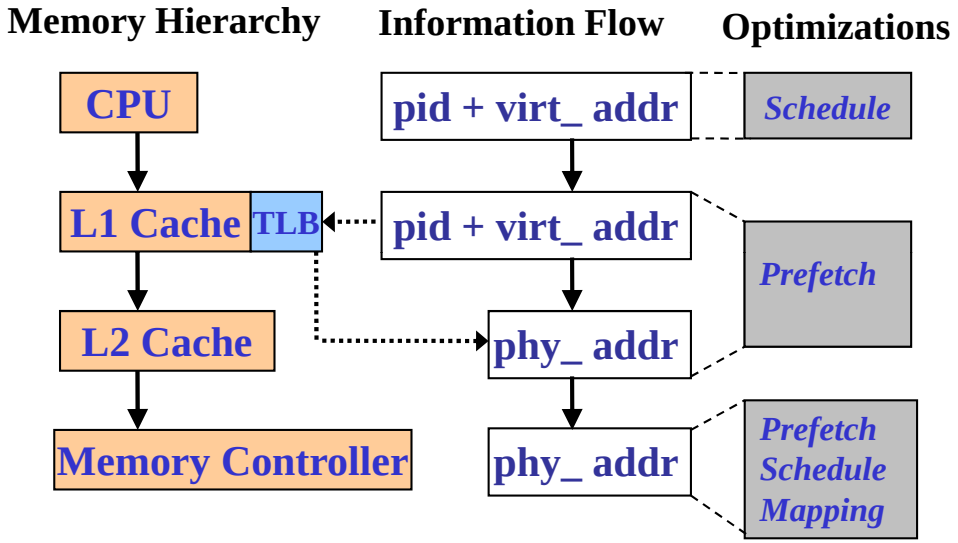
1.1 *Interleaved Memory Accesses*



Physical addresses are interleaved among multiple processes. Most proposed optimization techniques at memory controller level use only the interleaved addresses, and may not achieve same improvements in multicore platform, because they cannot differentiate address spaces of VMMs/processes.

1.2 *Information Flow in Memory Hierarchy*



In common memory hierarchy, while the hierarchy level increases, the information reduces. Only physical address survives after address translation.

2 Virtual Channel

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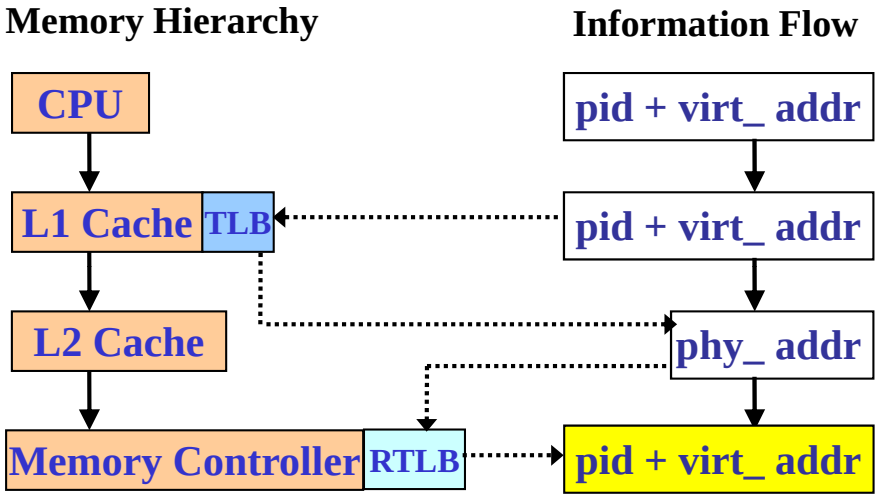
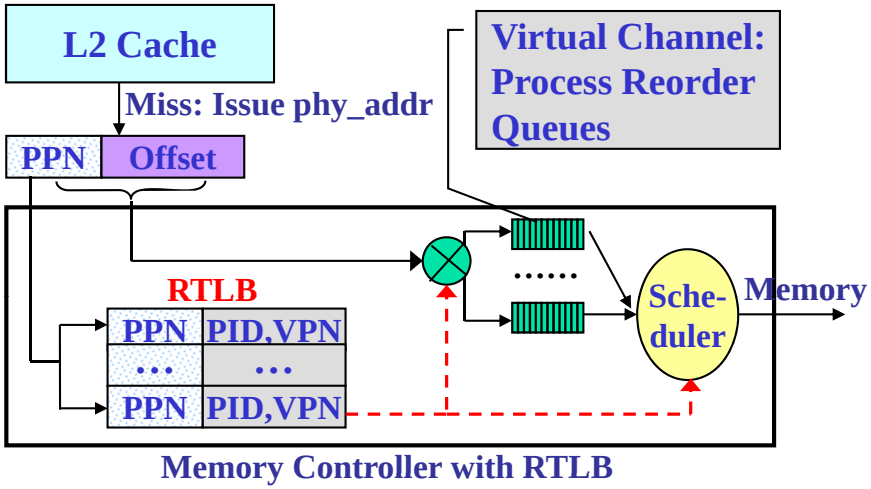
2.1 *Reverse-TLB (RTLB)*

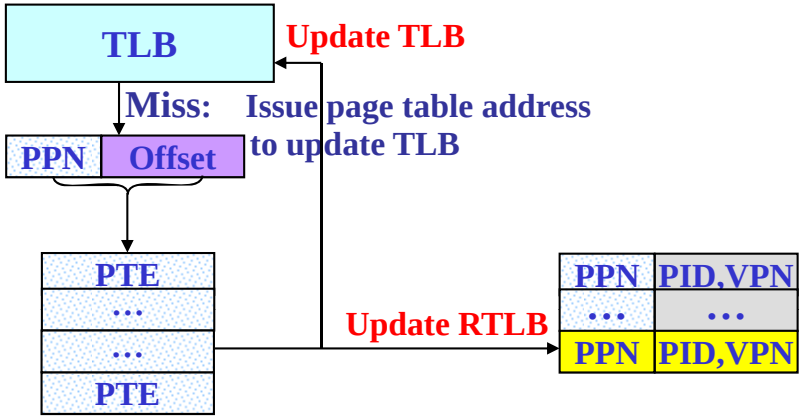


Reverse-TLB (RTLB) is introduced to support virtual channel mechanism for memory controller design, avoiding cache and program codes modification.

2.2 *Memory Controller Architecture*



2.3 *RTLB Update*



3 Experimental results

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3.1 Experimental Data Source

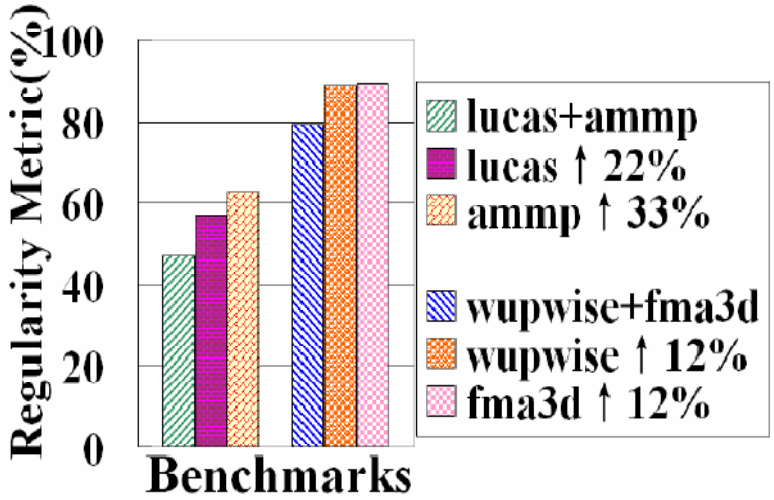
HMTT

\+ SPEC CPU2000

Trace *0*: wupwise
Trace *1*: fma3d
……
Trace *n*: lucas

Mixed multi-processes trace:
<timestamp, pid, virt_addr, r/w>

3.2 Virtual Channel helps explore more spatial regularity



Challenges

1. *How do RTLB and OS cooperate with each other for RTLB update and OS handling new memory controller events efficiently?;*
2. *How do VMM/OS/compiler use this information exposed by memory controller for schedule optimization?*
3. *How does memory controller use this more system information for optimizations?*